(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
31 December 2003 (31.12.2003)

PCT

(10) International Publication Number
WO 2004/001924 A1

(51) International Patent Classification[7]: H02H 3/33, 3/44

(21) International Application Number:
PCT/IE2003/000047

(22) International Filing Date: 25 March 2003 (25.03.2003)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
2002/0512 24 June 2002 (24.06.2002) IE

(71) Applicant *(for all designated States except US)*: SHAKIRA LIMITED [IE/IE]; Atreus Place, Poolboy, Ballinasloe, County Galway (IE).

(72) Inventor; and

(75) Inventor/Applicant *(for US only)*: WARD, Patrick [IE/IE]; Atreus Place, Poolboy, Ballinasloe, County Galway (IE).

(74) Agents: BOYCE, Conor et al.; F.R. Kelly & Co, 27 Clyde Road, Ballsbridge, Dublin 4 (IE).

(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZM, ZW.

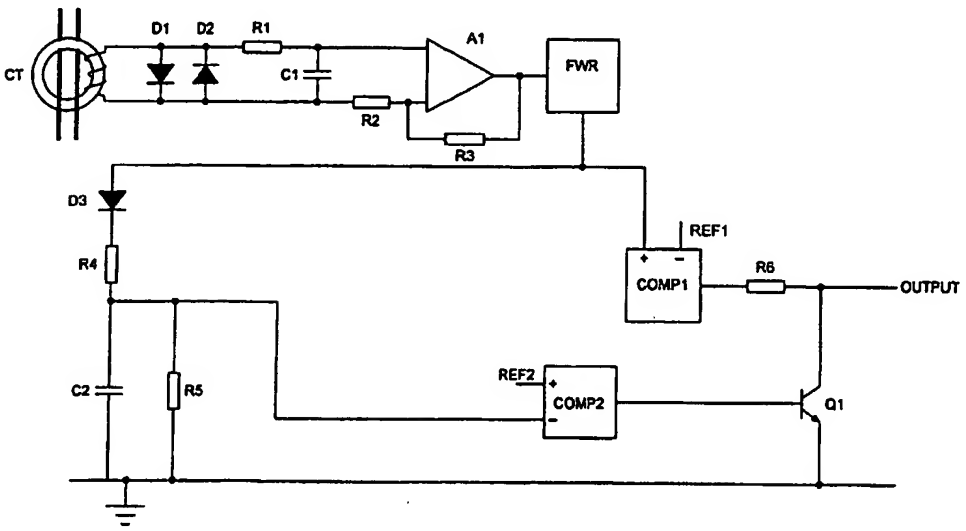
(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii)) for the following designations AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE,*

[Continued on next page]

(54) Title: RESIDUAL CURRENT DETECTION CIRCUIT



(57) Abstract: A residual current detection circuit comprises a current transformer CT for detecting an imbalance current indicative of a residual current and a full wave restifier FWR for providing an output whose amplitude corresponds to the magnitude of the residual current. The FWR output is applied simultaneously to two channels. The first channel includes a first comparator COMP1 to provide a first signal which persists during periods when the amplitude of the output exceeds a first level. The second channel includes a capacitor C2 which acquires a charge corresponding to the output level and a second comparator COMP2 for providing a second signal in response to the capacitor voltage exceeding a second level. An output is provided from the circuit only when the first signal is coincident with the second signal.

WO 2004/001924 A1